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06ES33

Third Semester B.E. Degree Examination, June/July 2014

Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Construct a truth table and write the Boolean output equations in canonical POS and SOP forms for the output P. P is to be true when the input variables x and y are true or when y is false but x and z are true. **(06 Marks)**

b. Simplify $T = w\bar{z} + xy\bar{z} + \bar{w}xy\bar{z} + \bar{w}xyz$ using K-map in POS form. **(06 Marks)**

c. Simplify R = f(a, b, c, d) = $\sum$m (2, 3, 4, 5, 9, 15) + dc (8, 10, 11, 13) using K-map and implement the circuit using NAND gates. **(08 Marks)**

2 a. Using Quine-Mc-Clusky's method, simplify the function,
f(A, B, C, D) = $\sum$m (0, 1, 5, 8, 9, 13, 14, 15). **(10 Marks)**

b. Simplify using VEM technique the following expression,
V = f(a, b, c, d) = $\sum$m (0, 1, 4, 8, 9, 10) + dc(2, 11) **(10 Marks)**

3 a. Realize the following functions using one 7418 decoder and extended gates:
P = f(x, y, z) = $\sum$(0, 4, 7)
Q = f(x, y, z) = $\sum$(3, 5, 6) **(08 Marks)**

b. Realize 4:16 decoder using 3:8 (74138) decoders. **(06 Marks)**

c. Write a note on priority encoder. **(06 Marks)**

4 a. Implement the expression $s = ad + b\bar{c} + bd$ using 4:1 mux. Choosing b and d as select lines. **(10 Marks)**

b. Design a full adder using gates. **(05 Marks)**

c. Design a one bit comparator. **(05 Marks)**

PART – B

5 a. Explain the operation of Gated SR latch. **(04 Marks)**

b. With the circuit diagram, explain the operation of pulse triggered Master Slave JK flip flop. **(06 Marks)**

c. With the circuit diagram, explain the working of positive edge triggered D flip flop. **(10 Marks)**

6 a. Derive the characteristic equation of T flip flop. **(02 Marks)**

b. Design a synchronous mod-6 counter using clocked JK flip flop with count sequence 0, 1, 2, 3, 4, 5, 0, ... in binary. **(10 Marks)**

c. With the function table and circuit, explain the operation of universal shift register. **(08 Marks)**

7 a. Write the Moore state model notation of JK flip flop. **(06 Marks)**

b. Write the characteristic equations, next state equation, output equation, transition table, excitation table, state table and state diagram for the circuit shown in Fig.Q7(b).

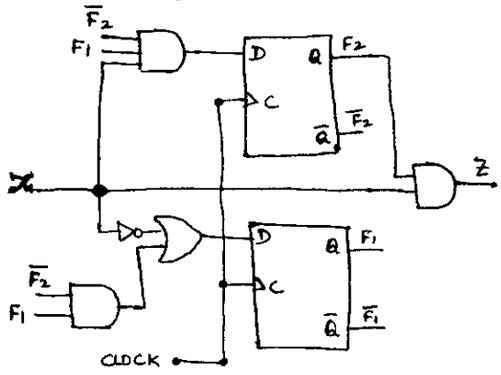

Fig.Q7(b) **(14 Marks)**

8 a. Construct the state diagram for a Mealy sequential circuit that will detect the serial input sequence x = 010110, when the complete sequence has been detected, then cause output z to go high. Assume the states as s_0, s_1, s_2, ... **(10 Marks)**

b. Design a modulo-8 synchronous binary counter using D flip flops that will count the number of occurrences of an input; that is, the number of times it is a '1', the input variable x must be coincident with the clock to be counted. The counter is to count in binary. Assume the flip flop inputs as D_3, D_2, D_1 and outputs as F_3, F_2, F_1 respectively. **(10 Marks)**

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